WHAT IS CLAIMED IS:

1. A method comprising

establishing at least two sequences of predetermined reference times on respective ones of at least two communication lines, at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences, and

encoding digital data onto data signals on one or more communication lines such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the communication lines is smaller than the time difference between the same data signal and the nearest one of the reference times on another one of the communication lines.

2. The method of claim 1 in which the reference times are rising or falling transitions of digital signals.

3. The method of claim 1 in which the data signals are at one of multiple potential time locations of rising or falling transitions of digital signals, where the multiple potential time locations comprise a data symbol.

4. The method of claim 3 wherein encoding comprises

associating a particular digital data value with one of the multiple potential rising transitions of the data symbol, and

associating a particular digital data value with one of the multiple potential falling transitions of the data symbol.

5. The method of claim 1 in which each of the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals.

6. The method of claim 5 wherein encoding comprises associating a particular digital data value with one of the multiple potential amplitude levels.

7. The method of claim 1 further comprising decoding the digital data based on the data signals and the sequences.

8. The method of claim 7 wherein decoding comprises delaying at least one of the sequences.
9. The method of claim 7 wherein decoding comprises delaying at least one of the data signals.
10. The method of claim 8 or claim 9 where decoding further comprises determining the order in time between one of the data signals and one of the reference times.
11. The method of claim 10 where decoding the digital data is based on the order in time.
12. An apparatus comprising

a source of at least two reference signals, each containing a sequence of predetermined reference times, at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences;

a modulator circuit having one or more outputs for data signals onto which digital data have been encoded such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the reference signals is smaller than the time difference between the same data signal and the nearest one of the reference times on another one of the reference signals, and at least two outputs for the reference signals;

a demodulator circuit with at least one input for the data signals and at least two inputs for the reference signals; and

a data bus comprising communication lines which are connected to both the modulator circuit and the demodulator circuit, which can enable the transmission of the data signals and the reference signals between the modulator and demodulator circuits.

13. The apparatus of claim 12 in which the reference times are rising or falling transitions of digital signals.
14. The apparatus of claim 12 in which the data signals are at one of multiple potential time locations of rising or falling transitions of digital signals, where the multiple potential time locations comprise a data symbol.
15. The apparatus of claim 14 where the modulator is configured to encode digital data onto the data signals by

associating a particular digital data value with one of the multiple potential rising transitions of the data symbol, and

associating a particular digital data value with one of the multiple potential falling transitions of the data symbol.

16. The apparatus of claim 12 in which each of the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals.

17. The apparatus of claim 16 where the modulator is configured to encode digital data onto the data signals by associating a particular digital data value with one of the multiple potential amplitude levels.

18. The apparatus of claim 12 in which the demodulator circuit is configured to decode the digital data based on the data signals and the reference signals.

19. The apparatus of claim 18 in which the demodulator circuit is further configured to delay at least one of the reference signals.

20. The apparatus of claim 18 in which the demodulator circuit is further configured to delay at least one of the data signals.

21. The apparatus of claim 19 or 20 in which the demodulator circuit is further configured to determine the order in time between one of the data signals and one of the reference times.

22. The apparatus of claim 21 in which the demodulator circuit is further configured to decode the digital data based on the order in time.

23. A system comprising

at least two integrated circuits mounted on at least one circuit board;

a data bus;

at least one modulator circuit;

at least one demodulator circuit;

a source of at least two reference signals, each containing a sequence of predetermined reference times, at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences;

the modulator circuit having one or more outputs for data signals onto which digital data have been encoded such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the reference signals is smaller than the

time difference between the same data signal and the nearest one of the reference times on another one of the reference signals, and at least two outputs for the reference signals;

the demodulator circuit with at least one input for the data signals and at least two inputs for the reference signals; and

the data bus comprising communication lines which are connected to both the modulator circuit and the demodulator circuit, which can enable the transmission of the data signals and the reference signals between the modulator and demodulator circuits.

24. The system of claim 23 in which the reference times are rising or falling transitions of digital signals.

25. The system of claim 23 in which the data signals are at one of multiple potential time locations of rising or falling transitions of digital signals, where the multiple potential time locations comprise a data symbol.

26. The system of claim 25 where the modulator is configured to encode digital data onto the data signals by

associating a particular digital data value with one of the multiple potential rising transitions of the data symbol, and

associating a particular digital data value with one of the multiple potential falling transitions of the data symbol.

27. The system of claim 23 in which each of the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals.

28. The system of claim 27 where the modulator is configured to encode digital data onto the data signals by associating a particular digital data value with one of the multiple potential amplitude levels.

29. The system of claim 23 in which the demodulator circuit is configured to decode the digital data based on the data signals and the reference signals.

30. The system of claim 29 in which the demodulator circuit is further configured to delay at least one of the reference signals.

31. The system of claim 29 in which the demodulator circuit is further configured to delay at least one of the data signals.

32. The system of claim 30 or 31 in which the demodulator circuit is further configured to determine the order in time between one of the data signals and one of the reference times.

33. The system of claim 32 in which the demodulator circuit is further configured to decode the digital data based on the order in time.